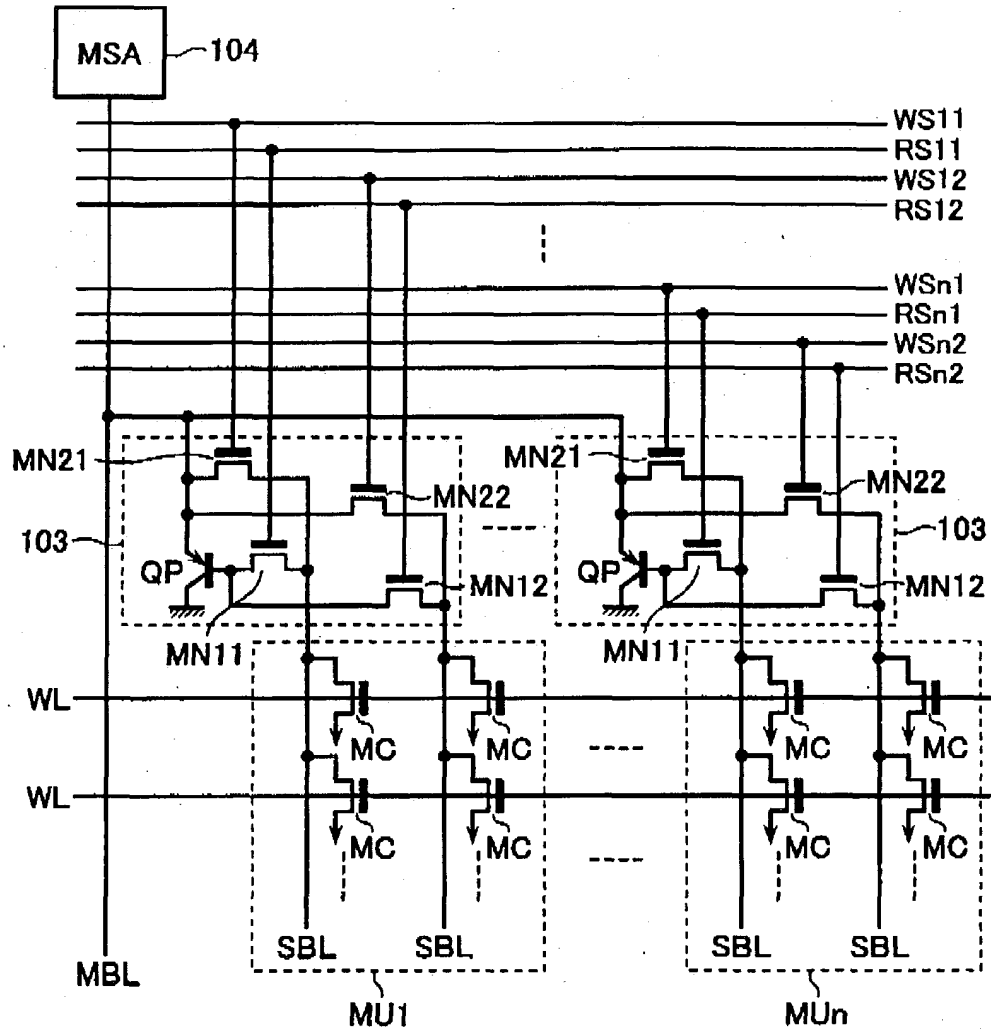


The diagram illustrates a memory array (101) and its sense amplifier (104). The sense amplifier (104) is connected to data lines Q and \bar{Q} and a word line D. It includes a latch (43) and two inverters (41 and 42). Transistors MP1 and MN3 are also present. The memory array (101) consists of multiple memory units (MU1 to MU_n). Each unit includes a BL Selector (102) and access transistors (MN1, MN2, MC). The array is controlled by word lines (WS1, RS1, WS_n, RS_n) and bit lines (WL, MBL). The sense amplifier (104) is connected to the array via a sense line (VBLR2) and a sense line (VSAR).

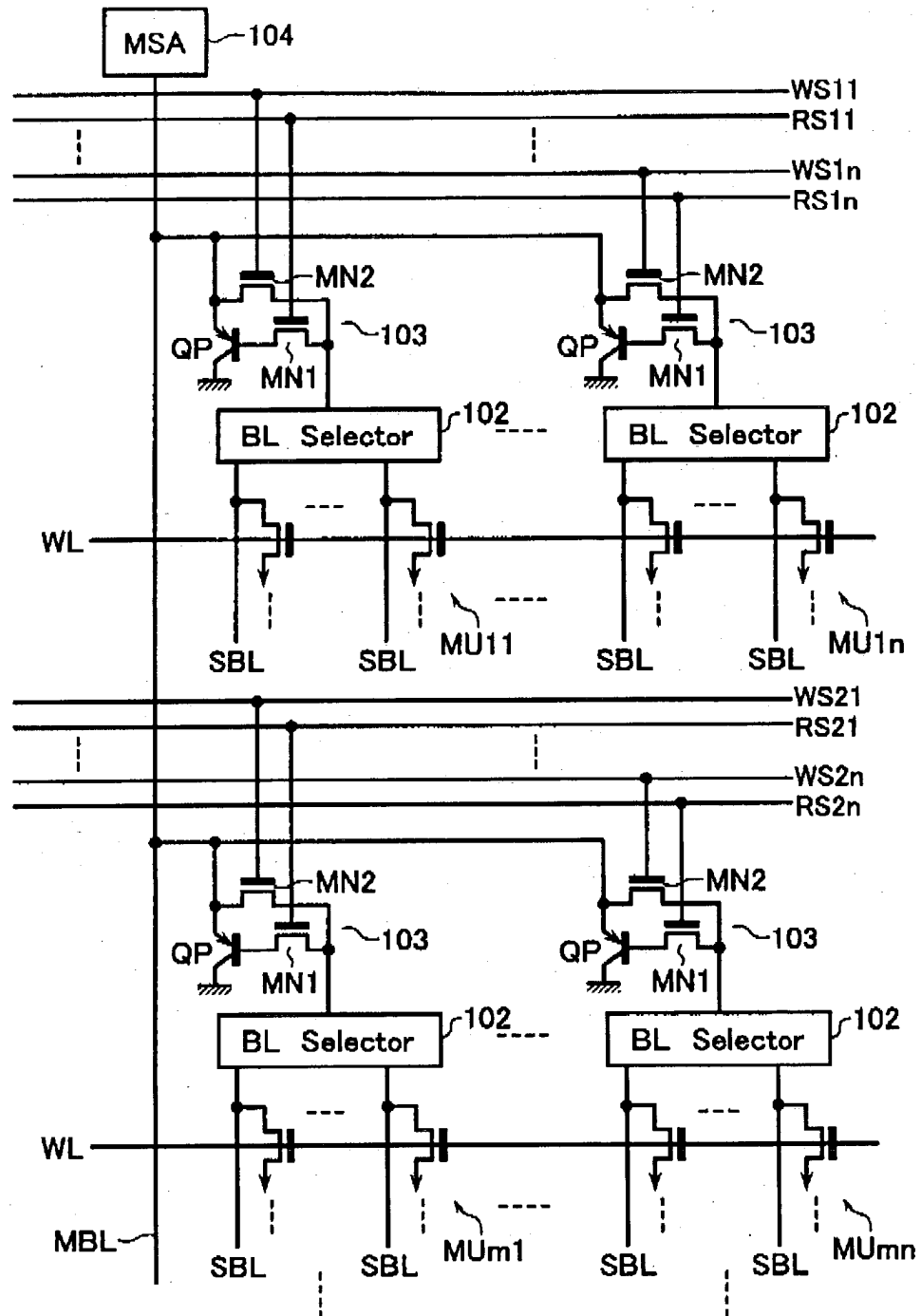
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FIG. 2



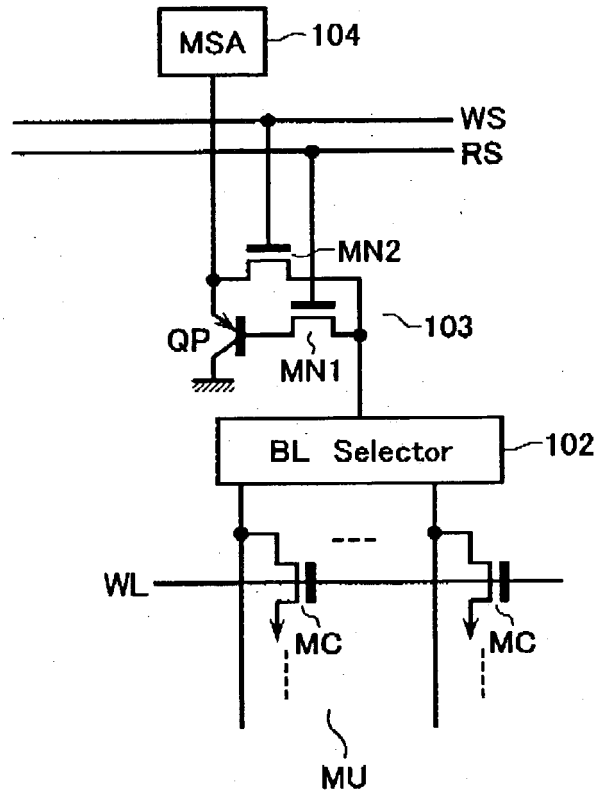
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FIG. 3



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FIG. 4



[illegible]

FIG. 6

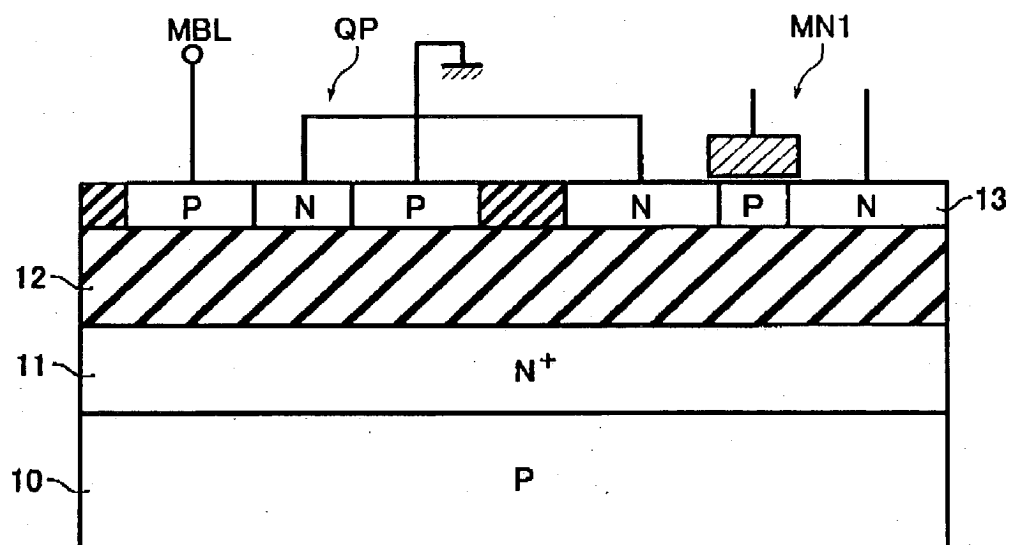
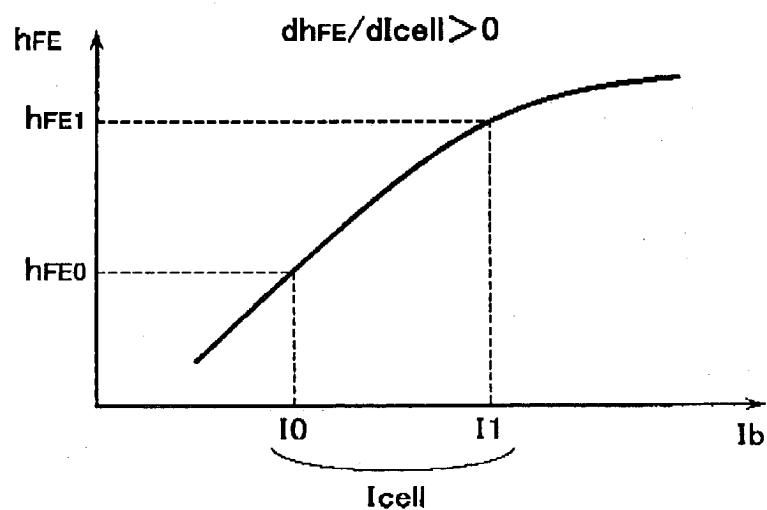


FIG. 7



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FIG. 8

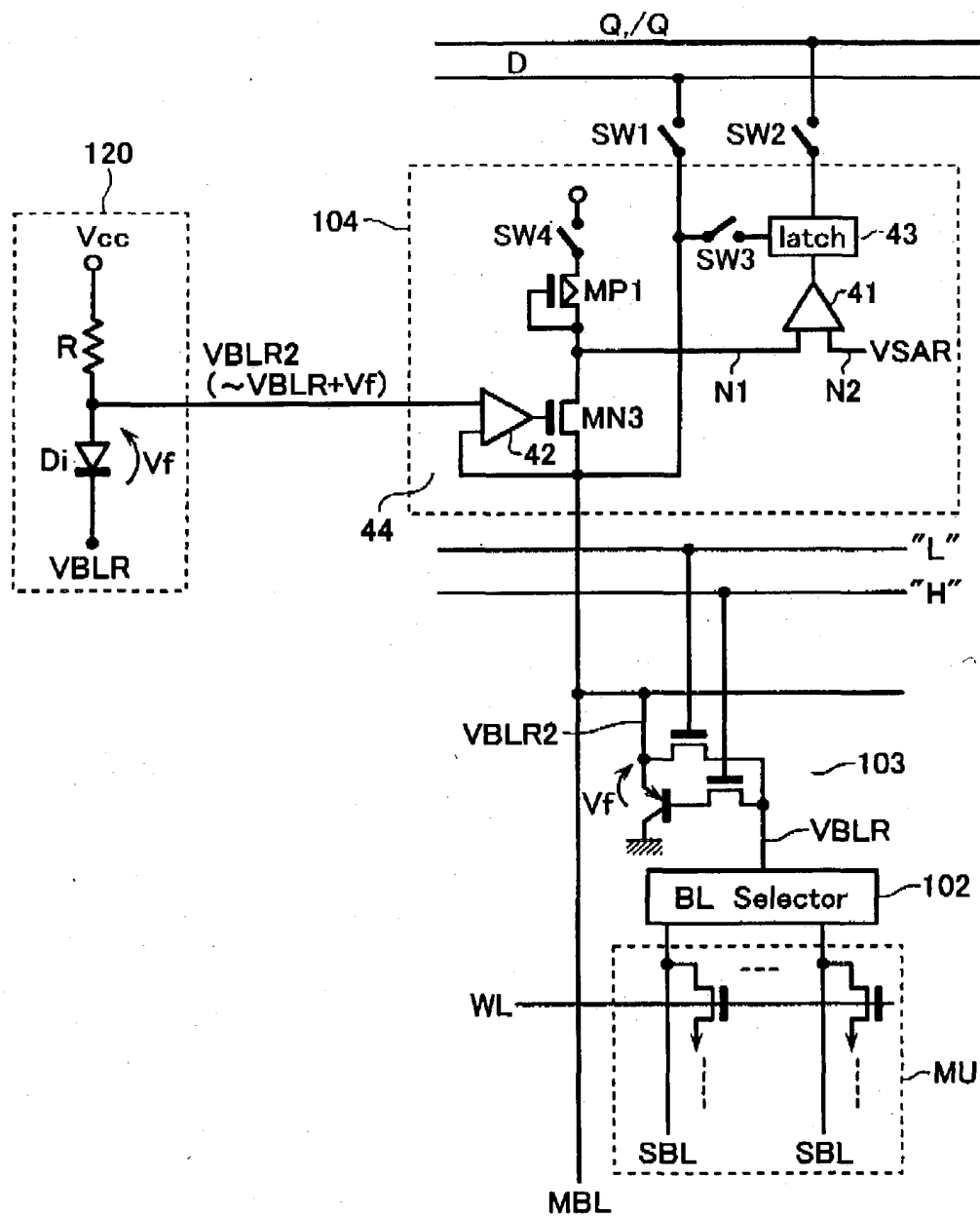
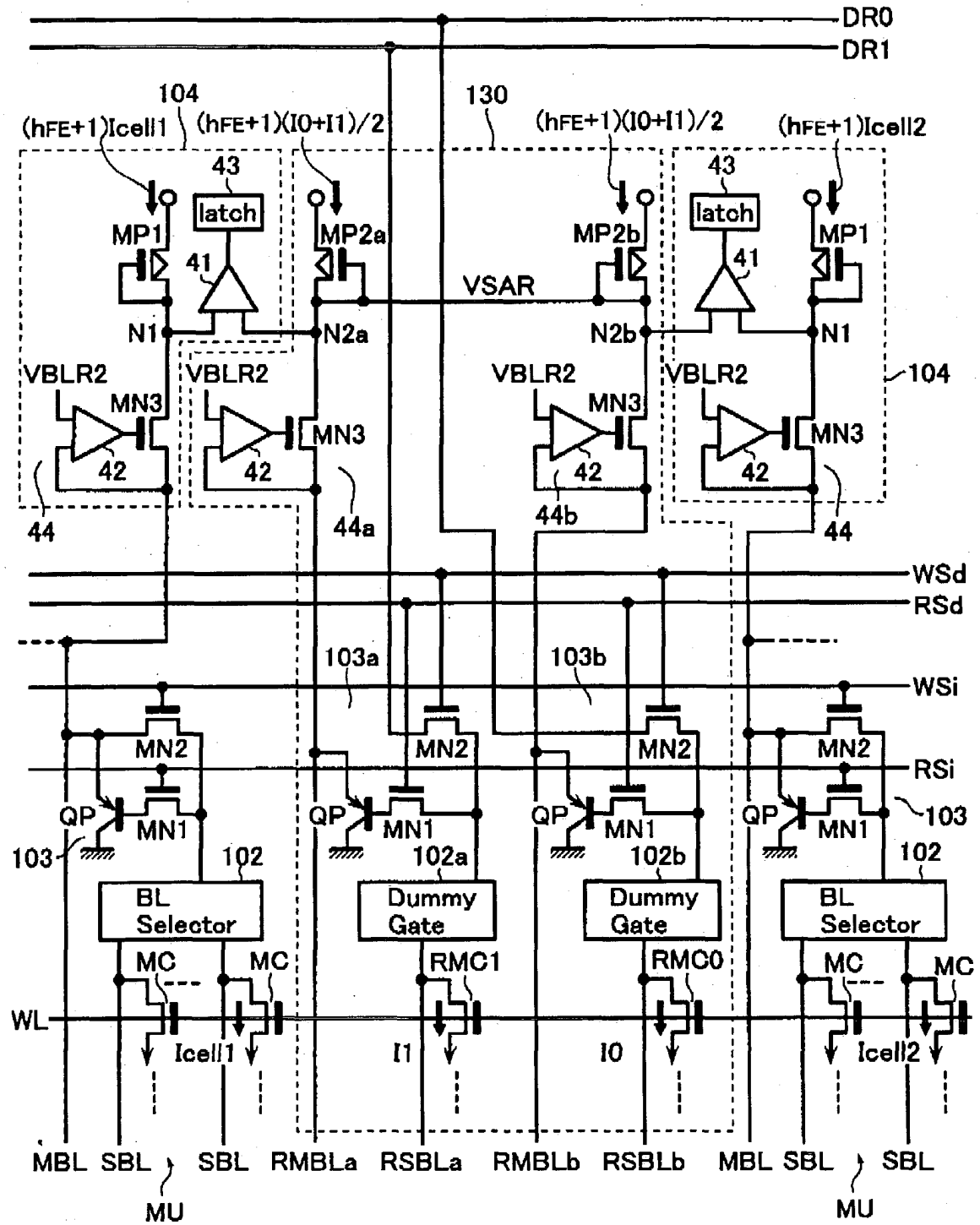


FIG. 9



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FIG. 10

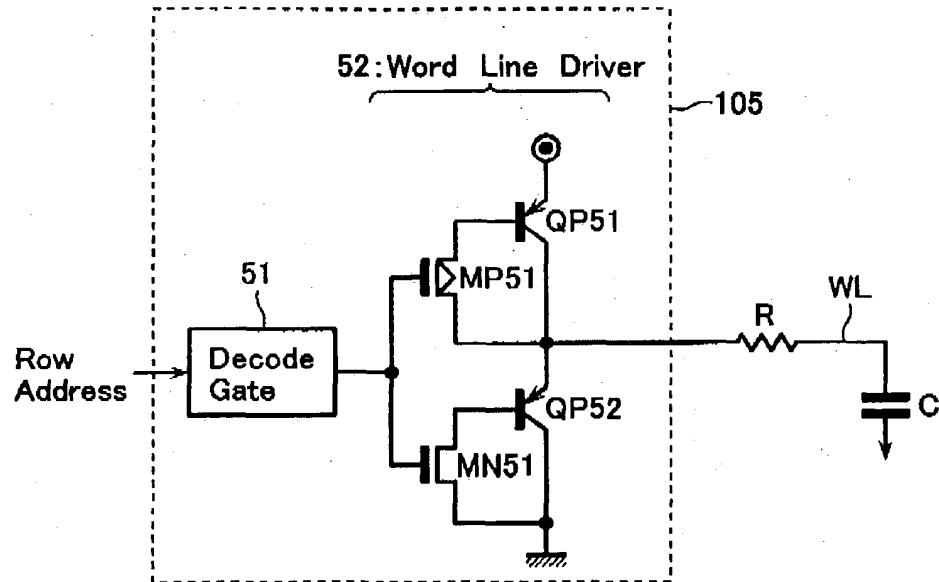
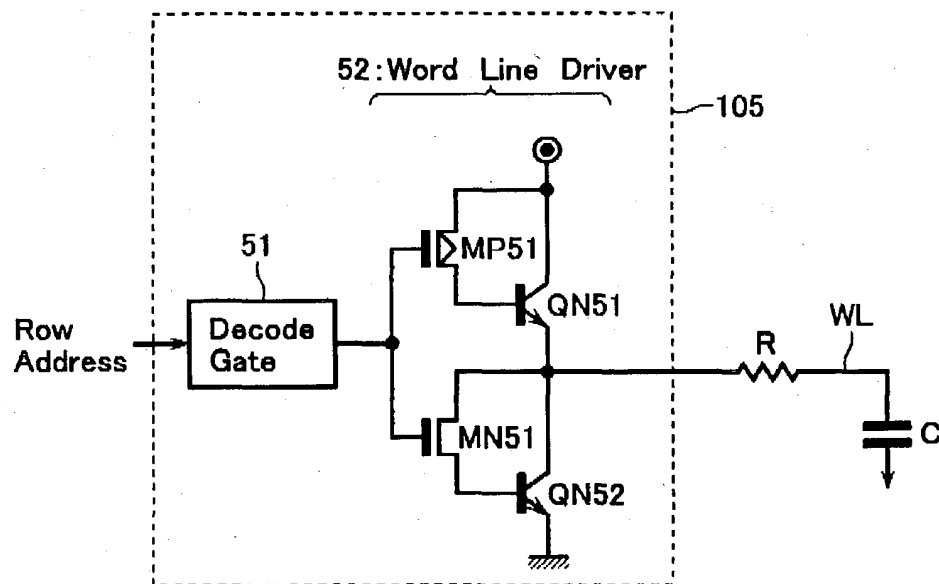


FIG. 11



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FIG. 12

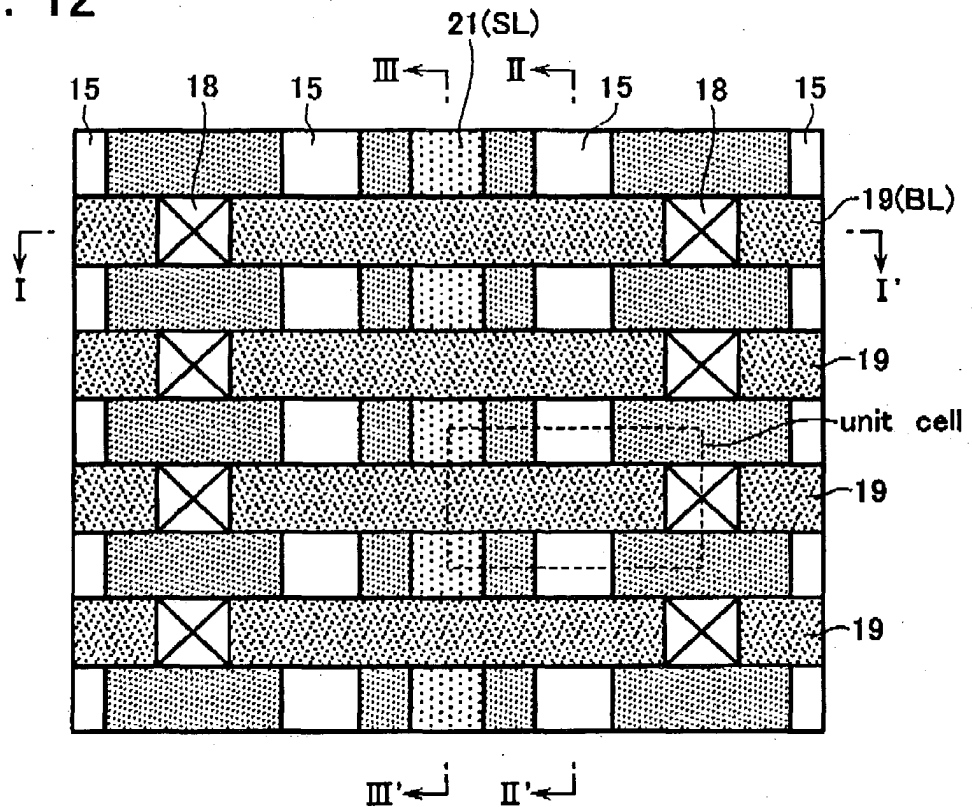
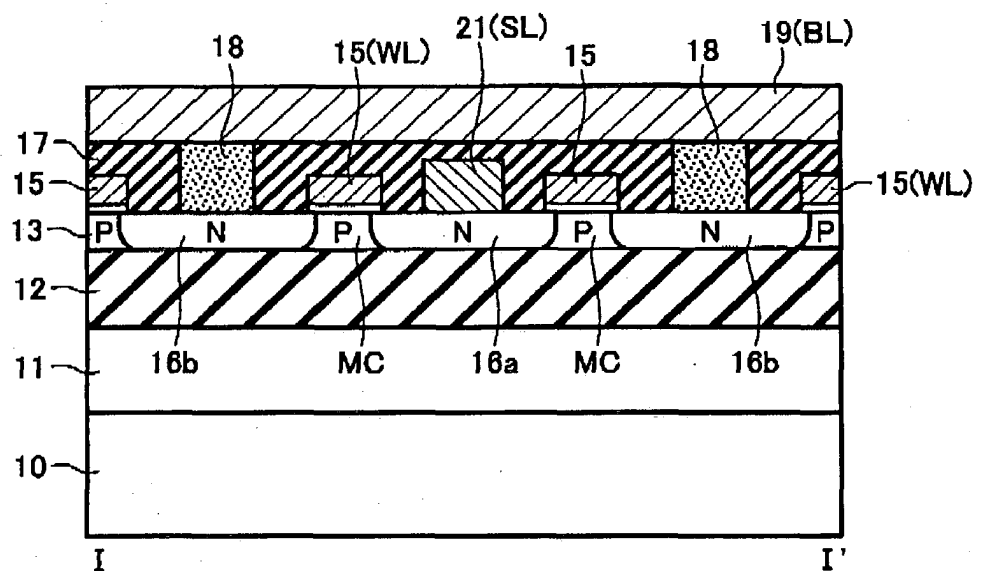


FIG. 13



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FIG. 14

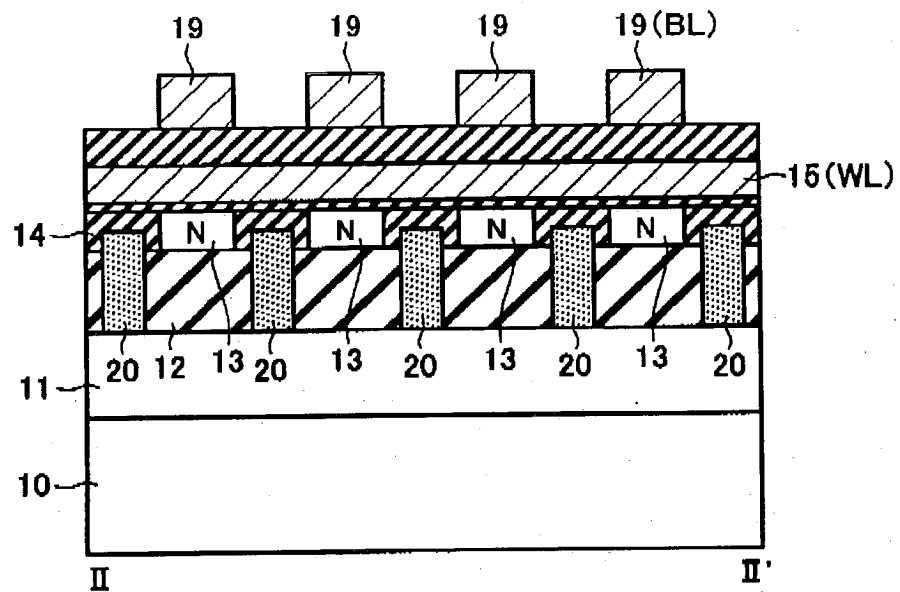
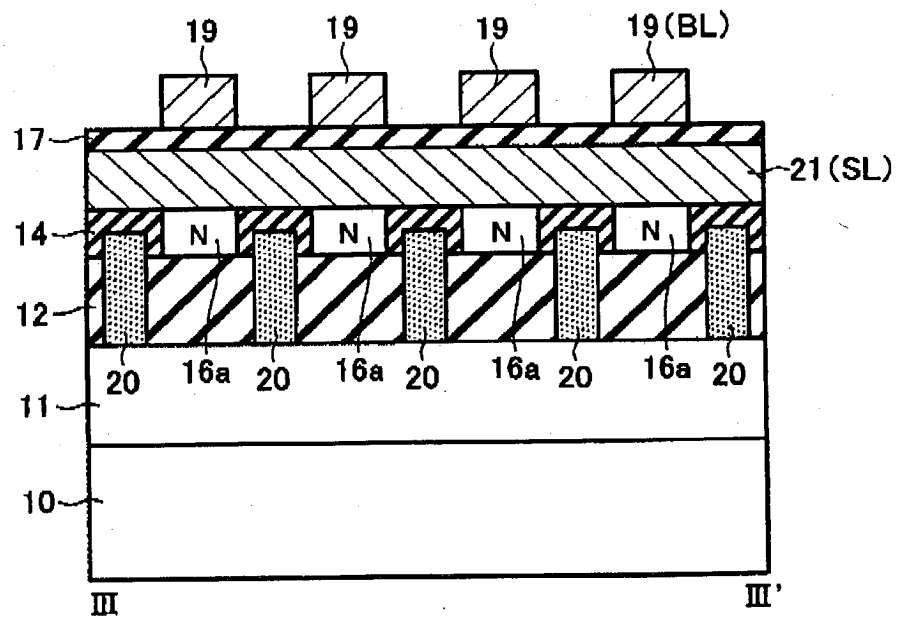


FIG. 15



[illegible]

FIG. 19

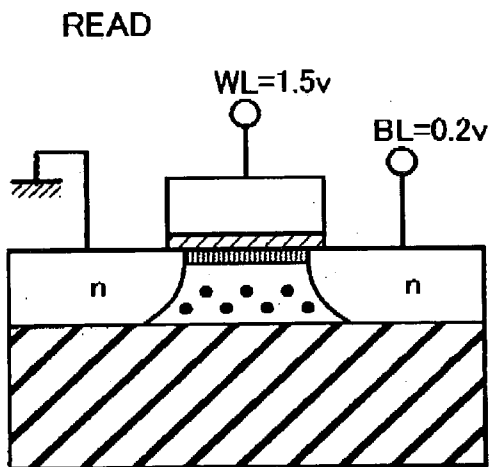


FIG. 20

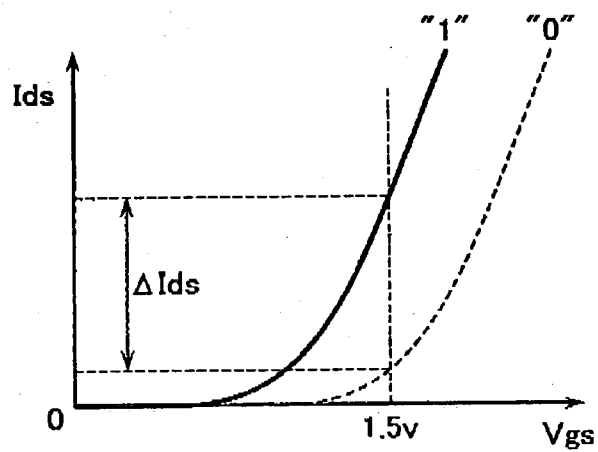
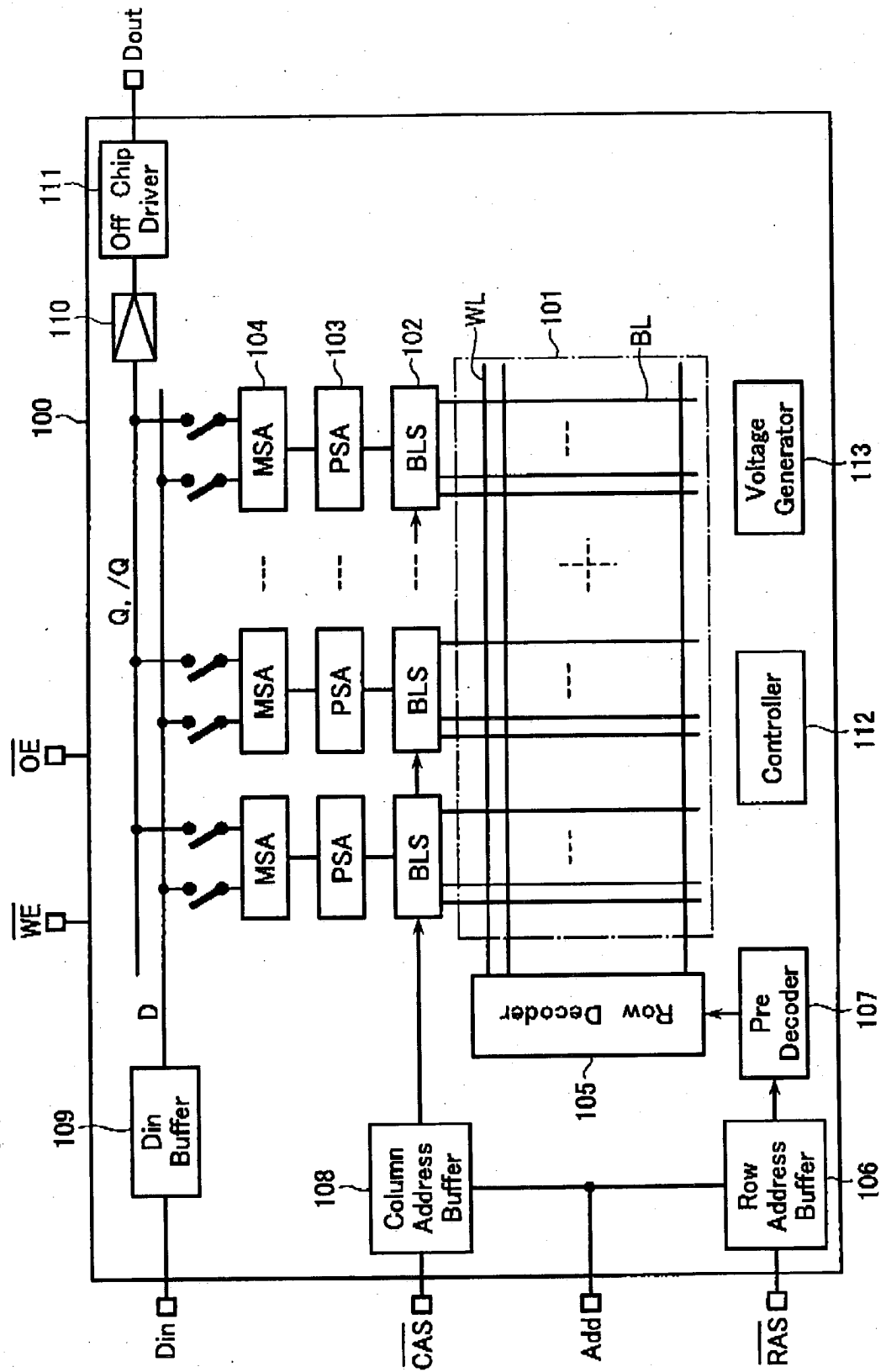


FIG. 21



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FIG. 22

